Dept Number	CS 504	Course Title	Testing of Integrated Circuits and Systems
Semester Hours	3	Course Coordinator	Bityut Gupta
Catalog Description	This course provides a detailed treatment of digital systems testing and testable design. Topics covered include fault modeling, fault simulation, testing for stuck faults, testing for bridging faults, delay faults, IDDQ faults, functional testing, built-in testing, design for testability, logic and system level diagnosis and PLA testing.		

Textbooks

References

Course Learning Outcomes

- Describe computer aided methodologies for testing the correctness of fabricated integrated circuits.
- Describe prefabrication computer aided design techniques that help established postfabrication testing methodologies.

Assessment of the Contribution to Program Outcomes

Outcome →	1	2	3	4	5	6	7	8	9	10
Assessed →	X	X	X	X	X		X			

Prerequisites by Topic

CS 401 and either 402 or consent of instructor

Major Topics Covered in the Course

1. Logic Simulation and Fault Modeling

   Types of simulation; delay models; hazard detection; fault detection, equivalence and dominance; single and multiple stuck faults {2 classes}
2. Fault Simulation

   Serial and parallel fault simulation; fault sampling and statistical fault analysis {2 classes}
3. Testing for Single Stuck Faults

   Fault oriented pattern generation; fault independent pattern generation; random test pattern generation; test pattern generation for sequential circuits {7 classes}
4. Testing for Bridging and IDDQ Faults

   The bridging fault model; detection, simulation and pattern generation for bridging faults; the IDDQ fault model; detection, simulation and pattern generation for IDDQ faults {4 classes}
5. Delay Faults

   Delay fault models; simulation and estimation; test pattern generation: enumerative and nonenumerative techniques {5 classes}
6. Functional Testing

   Functional testing without fault models: exhaustive and pseudoexhaustive testing; functional testing with specific fault models {2 classes}
7. Design for Testability Ad hoc techniques; scan designs; advanced scan concepts; board and system level approaches; boundary scan standards {6 classes}
8. Built-In Self Test: Pattern Generation and Compression

   Linear feedback shift registers; pseudoexhaustive and pseudorandom pattern generation; compression techniques and signature analysis; specific built-in self test architectures; advances in built-in self test {6 classes}
9. Logic and System Level Diagnosis

   Fault diagnosis for combinational circuits; models for system level diagnosis {3 classes}
10. PLA Testing

    Fault models; test generation algorithms; testable PLA designs {3 classes}